FORM PTO-1390 (Modified) (REV 11-98) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371

ATTORNEY'S DOCKET NUMBER	U.S. APPLICATION NO. (IF KNOWN, SEE 37 CFR
112740-321	09/936670

INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT/DE00/00641	01 March 2000	15 March 1999

TITLE OF INVENTION

METHOD AND APPARATUS FOR AUTOMATICALLY PRODUCING CLOCK SIGNALS FOR SAMPLING DATA SIGNALS AT DIFFERENT DATA RATES VIA A PHASE LOCKED LOOP

APPLICANT(S) FOR DO/EO/US

Fritz-Joerg Dauth

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. ☒ This is an express request to begin national examination procedures (35 U.S.C. 371(f)) at any time rather than delay examination until the expiration of the applicable time limit set in 35 U.S.C. 371(b) and PCT Articles 22 and 39(1).
4. ☒ A proper Demand for International Preliminary Examination was made by the 19th month from the earliest claimed priority date.
5. ☒ A copy of the International Application as filed (35 U.S.C. 371 (c) (2))
   a. ☒ is transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☐ has been transmitted by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US).
6. ☒ A translation of the International Application into English (35 U.S.C. 371(c)(2)).
7. ☒ A copy of the International Search Report (PCT/ISA/210).
8. ☒ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371 (c)(3))
   a. ☐ are transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☐ have been transmitted by the International Bureau.
   c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   d. ☒ have not been made and will not be made.
9. ☐ A translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
10. ☐ An oath or declaration of the inventor(s) (35 U.S.C. 371 (c)(4)).
11. ☒ A copy of the International Preliminary Examination Report (PCT/IPEA/409).
12. ☐ A translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371 (c)(5)).

Items 13 to 20 below concern document(s) or information included:

13. ☒ An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
14. ☐ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
15. ☒ A **FIRST** preliminary amendment.
16. ☐ A **SECOND** or **SUBSEQUENT** preliminary amendment.
17. ☒ A substitute specification.
18. ☐ A change of power of attorney and/or address letter.
19. ☒ Certificate of Mailing by Express Mail
20. ☒ Other items or information:

Submission of Drawings - Figures 1-2 on two sheets

531 Rec'd PCT/ 14 SEP 2001

U.S. APPLICATION NO. (IF KNOWN, SEE 37 CFR	INTERNATIONAL APPLICATION NO.	ATTORNEY'S DOCKET NUMBER
09/936670	PCT/DE00/00641	112740-321

21. The following fees are submitted:.

BASIC NATIONAL FEE (37 CFR 1.492 (a) (1) - (5)) :

		CALCULATIONS PTO USE ONLY
☐	Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2) paid to USPTO and International Search Report not prepared by the EPO or JPO	**$1,000.00**
☒	International preliminary examination fee (37 CFR 1.482) not paid to USPTO but Internation Search Report prepared by the EPO or JPO	**$860.00**
☐	International preliminary examination fee (37 CFR 1.482) not paid to USPTO but international search fee (37 CFR 1.445(a)(2)) paid to USPTO	**$710.00**
☐	International preliminary examination fee paid to USPTO (37 CFR 1.482) but all claims did not satisfy provisions of PCT Article 33(1)-(4)	**$690.00**
☐	International preliminary examination fee paid to USPTO (37 CFR 1.482) and all claims satisfied provisions of PCT Article 33(1)-(4)	**$100.00**

ENTER APPROPRIATE BASIC FEE AMOUNT =	**$860.00**	
Surcharge of **$130.00** for furnishing the oath or declaration later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492 (e)).	**$0.00**	

CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE		
Total claims	14 - 20 =	0	x $18.00	**$0.00**	
Independent claims	2 - 3 =	0	x $80.00	**$0.00**	
Multiple Dependent Claims **(check if applicable)**.			☐	**$0.00**	
TOTAL OF ABOVE CALCULATIONS			=	**$860.00**	
Reduction of 1/2 for filing by small entity, if applicable. Verified Small Entity Statement must also be filed (Note 37 CFR 1.9, 1.27, 1.28) **(check if applicable).**			☐	**$0.00**	
SUBTOTAL			=	**$860.00**	
Processing fee of **$130.00** for furnishing the English translation later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492 (f)).			+	**$0.00**	
TOTAL NATIONAL FEE			=	**$860.00**	
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31) **(check if applicable).**			☐	**$0.00**	
TOTAL FEES ENCLOSED			=	**$860.00**	
				Amount to be: refunded	$
				charged	$

☒ A check in the amount of **$860.00** to cover the above fees is enclosed.

☐ Please charge my Deposit Account No. in the amount of to cover the above fees.
A duplicate copy of this sheet is enclosed.

☒ The Commissioner is hereby authorized to charge any fees which may be required, or credit any overpayment to Deposit Account No. **02-1818** A duplicate copy of this sheet is enclosed.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

SEND ALL CORRESPONDENCE TO:

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SIGNATURE

William E. Vaughan
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39,056
REGISTRATION NUMBER

September 14, 2001
DATE

BOX PCT

IN THE UNITED STATES ELECTED/DESIGNATED OFFICE

OF THE UNITED STATES PATENT AND TRADEMARK OFFICE

UNDER THE PATENT COOPERATION TREATY-CHAPTER II

PRELIMINARY AMENDMENT

APPLICANT:	Fritz-Joerg Dauth	DOCKET NO: 112740-321
SERIAL NO:		GROUP ART UNIT:
		EXAMINER:
INTERNATIONAL APPLICATION NO:		PCT/DE00/00641
INTERNATIONAL FILING DATE:		01 March 2000
INVENTION:	METHOD AND APPARATUS FOR AUTOMATICALLY PRODUCING CLOCK SIGNALS FOR SAMPLING DATA SIGNALS AT DIFFERENT DATA RATES VIA A PHASE LOCKED LOOP	

Assistant Commissioner for Patents,
Washington, D.C. 20231

Sir:

Please amend the above-identified International Application before entry into the National stage before the U.S. Patent and Trademark Office under 35 U.S.C. §371 as follows:

In the Specification:

Please replace the Specification of the present application, including the Abstract, with the following Substitute Specification:

SPECIFICATION

TITLE OF THE INVENTION

METHOD AND APPARATUS FOR AUTOMATICALLY PRODUCING CLOCK SIGNALS FOR SAMPLING DATA SIGNALS AT DIFFERENT DATA RATES VIA A PHASE LOCKED LOOP

BACKGROUND OF THE INVENTION

The high level of transparency of optical networks with regard to data transmission rates and the use of different transmission methods and transmission protocols for the transmission of digital information (for example, the Synchronous Digital Hierarchy SDH, Gigabit-Ethernet, Fiber Channel) requires future devices for data regeneration and for reproduction of the amplitude, flank and clock of a transmitted digital data signal or data stream - also referred to as "3R data regeneration".

Apparatuses for producing a clock signal from a digital data stream or from a data signal stream are known. Phase/frequency control loops or phase locked loops are frequently used for clock recovery and include, for example, a phase discriminator, a frequency discriminator, a loop filter, voltage controlled oscillators (also referred to as VCOs) and variable digital frequency dividers. The function of phase locked loops for clock recovery from a digital data stream and for sampling of the digital data stream to be regenerated via a sampling flipflop are sufficiently well known to those skilled in the art, such that their method of operation will not be described in further detail.

Various methods for determining the data transmission rate of the digital data stream are used to preset the phase locked loop. All the methods used, in particular, in wide area networks or WAN communications networks are based on more or less exactly determining the statistically distributed flank changes in the data stream within a defined observation time period. Conclusions can be drawn on the actual data transmission rate from the number of flank changes identified. These methods are also referred to as flank density analyses. Apart from the described flank density analysis, period duration measurements of individual bits are also used for low transmission rates.

By way of example, Laid-Open Specification DE 197 04 299 A1 describes an apparatus for producing a clock signal from a data signal, and a bit rate identification device for determining the bit rate of the incoming data signal. The apparatus includes a phase/frequency control device and a frequency divider device

which is arranged in the feedback part of the phase/frequency control device and can be switched via a data word. The switchable frequency divider device is connected to the bit rate identification device, to which the digital data stream and at least one reference frequency signal can be supplied. The bit rate identification device provides a bit-rate-dependent data word as a function of the applied reference frequency signal and the digital data stream passed to it. This is then supplied to the frequency divider device arranged in the phase/frequency control device. The described apparatus for producing a clock signal from a digital data signal or data stream has the disadvantage that the resolution of the identification circuit is highly limited; that is, digital data stream transmission rates which differ by less than a factor of 4 cannot be distinguished reliably in this way. A further disadvantage is the risk of false synchronization to side lines in the frequency spectrum during the transmission of certain data contents, for example, when transmitting AIS information in SDH signals (Synchronous Digital Hierarchy).

The present invention is, therefore, directed toward improving the production of a clock signal from a transmitted digital data signal during a synchronization process and, in particular, the synchronization of the clock signal to the incoming digital data signal.

SUMMARY OF THE INVENTION

The method according to the present invention provides for automatic production of clock signals for sampling data signals at different data rates via a phase locked loop. A major aspect of the method according to the present invention is that, during a synchronization process, the data signal is sampled successively using a clock signal at different frequencies, which are associated with different transmission protocols, and is checked for the presence of protocol identification information associated with the selected clock signal, until protocol identification information is detected.

A major advantage of the method according to the present invention is that the link between the detection of the transmission rate of the transmitted digital data signal and the detection of the transmission protocol that is matched to the

frequency of the digital data signal or of the clock signal that is produced avoids false synchronization of the clock signal that is produced to side lines, harmonics and subharmonics of the transmission frequency or transmission rate of the data signal. The method according to the present invention also makes it possible to distinguish reliably between transmission rates that are arranged adjacent in the frequency domain, for example, distinguishing between "Gigabit-Ethernet" at a transmission rate of 1.25 Gbit/s and "Fiber Channel" at a transmission rate of 1.064 Gbit/s. A further advantage of the method according to the present invention is that it allows the transmission rate to be set automatically to "3R data regeneration" for frame-oriented transmission methods, and automatic identification of the respective transmission protocol. In future optical communication networks, the method according to the present invention will allow not only pure wavelength conversion via flexible "3R data regeneration", but also analysis of the respectively transmitted digital data signals or data streams, for example, for the preprocessing of statistics, in order to provide network planning, or for volume-dependent billing.

Additional features and advantages of the present invention are described in, and will be apparent from, the following Detailed Description of the Invention and the Figures.

BRIEF DESCRIPTION OF THE FIGURES

Figure 1 shows a circuit arrangement for producing a clock signal, according to the present invention, from a transmitted digital data stream.

Figure 2 shows an example of a tabular representation of the binary information which is required to carry out the method according to the present invention and is stored in a memory in the circuit arrangement.

DETAILED DESCRIPTION OF THE INVENTION

Figure 1 uses a block diagram to show an exemplary embodiment of a circuit arrangement for producing a clock signal ts from a digital data signal or data stream ds passed to it. The circuit arrangement illustrated in Figure 1 is subdivided into two functional circuit units PLL, RD, which are each represented by a rectangle with a dashed-dotted outline. The first functional circuit unit includes a

phase/frequency control device (PLL), which is generally known to those skilled in the art and is also referred to as a phase locked loop or PLL circuit. The second circuit unit includes a frame identification RD, which is connected to the phase/frequency control device (PLL) and is also referred to in the following text as frame detector.

A digital data stream ds transmitted with the aid of a transmission protocol is passed to one input ET of the phase/frequency control device PLL and is passed on to an input EF of a sampling flipflop AFF. In the exemplary embodiment, it is assumed that the data stream ds is transmitted in accordance with the Synchronous Digital Hierarchy SDH. The Synchronous Digital Hierarchy is based on synchronous transmission of user information using synchronous transport modules (also referred to as STM) with a standard structure. The basic transport module is the STM-1 frame, with a data transmission rate of 155 Mbit/s. Each STM-1 frame includes a matrix of 9 rows each having 270 data octets. The frame has a repetition frequency of 125 µs, and the transmission is carried out at a bit rate of 155.520 Mbit/s. The STM-1 frame is inserted into a payload and an overhead, with the first 9 octets in all 9 rows containing the overhead, and the remaining columns containing the payload. The overhead contains information which is required to operate SDH systems, and these are also referred to as section overheads (SOH) and are transported in the SOH areas of the overhead. The SOH areas contain, for example, the A1 and A2 bytes, which are known to those skilled in the art, and which each represent frame identification information.

The data input ET of the phase/frequency control device PLL is at the same time connected to a first input EP of a discriminator unit DE. A reference signal f_{Ref} at a reference frequency is passed to a second input EF of the discriminator unit DE. The discriminator unit DE is functionally subdivided into two components, a phase discriminator PD and a frequency window discriminator FD, each indicated by a rectangle with a dashed outline.

The discriminator unit DE is connected via an output AP to an input EL of a loop filter LF, which is, in turn, connected via an output AL to an input EV of a

voltage controlled oscillator VCO. A first and a second variable digital frequency divider T1,T2 is each connected via an input ET to an output AV of the voltage controlled oscillator VCO. The first digital frequency divider T1 is connected to a clock input CLK of the phase discriminator PD, and the second digital frequency divider T2 is connected to a divider input ETF of the frequency window discriminator FD, in each case via an output AT. The described discriminator unit DE, including a phase window discriminator PD and a frequency window discriminator FD, as well as the loop filter LF, the voltage controlled oscillator VCO and the two variable digital frequency dividers T1, T2 are functional components of a generally known phase locked loop, whose function for recovery of the clock from the data stream ds passed to it in addition to the sampling of the data stream ds to be regenerated in conjunction with the sampling flipflop AFF are sufficiently well known to those skilled in the art, and will not be described in any more detail in the following text.

The phase/frequency control device PLL has a clock output CA which is connected to the output AT of the first frequency divider T1, and to which the clock signal ts which is produced is passed. The output AT of the first frequency divider T1 is, in turn, connected to a clock input CLK of the sampling flipflop AFF. The sampling flipflop AFF is connected via an output AF to a data output AT of the phase/frequency control device PLL, to which the data stream cds, regenerated via the sampling flipflop AFF, is passed. Furthermore, the output AF of the sampling flipflop AFF is connected to an input ES of a shift register SR arranged in the frame identification unit RD. The shift register SR has a clock input CLK which is connected to the output AT of the first frequency divider T1.

Furthermore, a memory MEM is arranged in the frame identification unit RD and is connected via a connecting line to a control unit STRG arranged in the frame identification unit RD. A table tab, illustrated in Figure 2, is stored in the memory MEM. The illustrated table tab has a number of table entries te1...n, with each table entry te1...n having a respectively associated, defined transmission protocol. Each table entry te1...n is used to store protocol identification information

PID1...n which uniquely identifies the respectively defined transmission protocol (for example, the frame identification information contained in the overhead information, in this case the A1 and A2 bytes) control loop control information PLL_WORD1...n for setting the phase/frequency control device PLL to the transmission rate to be expected for the data stream ds, and further overhead control information CNT_WD1...n for optional protocol-specific evaluation and processing of the overhead information arranged in the respective data packets or data frames of the data stream ds, cds. The overhead control information CNT_WD1...n can be used to evaluate, and if necessary to recalculate, for example, the B1 byte contained in the overhead information in a data stream transmitter using the SDH transmission method.

The control unit STRG is connected via a data bus DB having a number of data lines to a memory register MR, which is arranged in the frame identification unit RD and to which protocol identification information PID1...n which is stored in the memory MEM can be transmitted and stored therein, indicated by a rectangle with a dashed outline. The shift register SR and the memory register MR are connected via respective outputs AS, AM and a respective number of data lines DL1...n to corresponding inputs EC of a comparator unit COMP. The comparator COMP has comparison capabilities which are used to compare the binary information or data words applied to the inputs EC, and the comparison result is transmitted in the form of a data signal int via an output AC and a signaling line SCS to an input ES of the control unit STRG.

The data bus DB is also used to connect the control unit STRG to a register unit REG, which is connected via first outputs A1 and via first control lines SL1 to a control input S of the frequency window discriminator FD, via second outputs A2 and via second control lines SL2 to corresponding control inputs S of the second controllable frequency divider T2, via third outputs A3 and third control lines SL3 to corresponding inputs S of the first controllable frequency divider T1, and via fourth outputs A4 and fourth control lines SL4 to corresponding inputs S of the voltage controlled oscillator VCO. The register unit REG has one or more memory

registers (Figure 1 shows only one memory register, in the form of a rectangle with a dashed outline) in each of which the control device control information PLL_WORD1...n stored in the memory MEM, or control words or binary information derived from such control information, can be stored, via which the circuitry components, in this case FD, PD, LF, VCO, T1 and T2, arranged in the phase/frequency control device PLL can be controlled. Alternatively, analog signals can be derived from the control words stored in the register REG, and can be supplied to the circuitry components.

The frame identification unit RD also has a control/monitoring interface SS, which is connected to the control unit STRG via a connecting line.

The method, which can be implemented via the circuit arrangement illustrated in Figure 1, for producing a clock signal ts from the digital data stream ds transmitted with the aid of a transmission protocol optionally allows both the manual and automatic selection of a transmission protocol, and corresponding presetting of a data transmission rate matched to the selected transmission protocol. The method for producing the clock signal ts on the basis of manual selection, also referred to as a manual operating mode, and on the basis of automatic selection, also referred to as an automatic operating mode - of the transmission protocol and of the associated data transmission rate is explained in more detail in the following text with reference to the circuit arrangement illustrated in Figure 1. For the further exemplary embodiment, it is assumed that the digital data stream ds is transmitted with the aid of a frame-oriented transmission protocol, in this case STM-1, to the input ET of the phase/frequency control device (PLL) and is passed on to the data input EF of the sampling flipflop AFF.

Manual operating mode

During manual operation of the circuit arrangement, the transmission protocol with which the digital data stream ds is transmitted to the data input EF of the sampling flipflop AFF is known. On the basis of the knowledge of the transmission protocol, the control unit STRG arranged in the frame identification unit RD selects the first table entry te1 that is associated with the STM-1

transmission protocol in the table tab and reads the corresponding control loop control information, in this case PLL_WORD1, from the memory MEM, and transmits this via the data bus DB to the corresponding register or registers in the register unit REG. Alternatively, further control information can be derived from the transmitted control loop control information PLL_WORD, and can be stored in the corresponding register in the register unit REG. According to a further embodiment (not illustrated) a number of control words or control device control information items associated with the STM-1 transmission protocol also can be stored in the respective table entries te1...n in the table tab (not illustrated in Figure 2), which are transmitted via the data bus DB to corresponding registers in the register unit REG. The transmission of the control loop control information PLL_WORD1...n stored in the memory MEM allows the circuitry components VCO, T1, T2, FD, PD, LF to be preset to the corresponding data transmission rate of the incoming digital data stream ds_1 in this case 155 Mbit/s. Furthermore, the control unit STRG reads the protocol identification information, in this case PID1, associated with the selected transmission protocol, in this case STM-1, from the corresponding table entry te1 in the table tab, and transmits this via the data bus DB to the memory register MR, in which it is temporarily stored. In this exemplary embodiment, the frame identification word which is specific for the STM-1 transmission protocol and includes the last A1 and the first A2 byte of the overhead information is transmitted as the protocol identification information PID1 to the memory register REG.

As already explained, the phase locked loop which is arranged in the phase/frequency control device PLL is matched to the data transmission rate of the incoming digital data stream ds via the control loop control information PLL_WORD1 stored in the register unit REG. By way of example, the transmission of appropriate control information si2,3 via the control lines SL2 and SL3 sets the controllable frequency dividers T1, T2 such that the frequency of the signal delivered from the voltage controlled oscillator VCO is divided as appropriate for matching of the optimum operating point of the phase discriminator PD and of the

frequency window discriminator FD. Additional control information, in this case si4, transmitted via the fourth control line SL4 is used to provide any possibly required presetting or switching of the voltage controlled oscillator VCO. According to one alternative embodiment of the circuit arrangement, a number of voltage controlled oscillators VCO can be arranged in the phase/frequency control device PLL, in which case one voltage controlled oscillator VCO, which is matched to the data transmission rate of the incoming digital data stream ds, in each can case be selected with the aid of the fourth control signal si4.

According to a further embodiment of the circuit arrangement, which is not illustrated in Figure 1, the loop filter LF arranged in the phase/frequency control device PLL is likewise controlled as a function of the control loop control information PLL_WORD1...n stored in the register unit REG.

The digital data stream cds sampled with the aid of the recovered clock signal ts is read to the shift register SR, that is to say the shift register SR contains the data bits read with the aid of the recovered clock ts. Alternatively, the data stream ds which is applied to the input ET but is not sampled also can be read to the shift register SR, which is clocked by the clock signal ts, via a connecting line, indicated by a dashed connecting line in Figure 1.

The bit sequence read to the shift register SR is permanently compared by the comparator unit COMP with the protocol identification information, in this case pid1, temporarily stored in the memory register MR. If the comparator unit COMP finds a match or a partial match between the digital bit sequence that is read and the protocol identification information pid1, a corresponding control signal int is generated in the comparator unit COMP, and is transmitted via the control line SCS to the control unit STRG. The transmission of the control information int to the control unit STRG indicates the identification of the selected transmission protocol, in this case STM1, and the setting of the associated data transmission rate for the phase/frequency control device PLL.

In order to improve the synchronization of the clock signal ts that is produced to the incoming digital data stream ds, according to a further embodiment

that is not illustrated, the control unit STRG checks whether the protocol identification information, in this case pid1, is identified more than once, for example three times, in a cycle time which is specific for the selected transmission protocol. If the transmission protocol being used resulting the frame sequence being asynchronous, for example when using the Gigabit-Ethernet transmission protocol, this embodiment allows the pause pattern, or "Interframe Gap", to be analyzed.

When the selected or expected protocol identification information pid1 is identified in the sampled data stream cds, the start of data transmission can be recorded via the control unit STRG. If there are no periodically produced data frames, for example when using the STM-1 transmission protocol, it is advantageously possible in conjunction with further parameters, for example loss of the signal (LOS) or optical level, to deduce that there is a fault or that this is the end of transmission. In the situation where the phase locked loop which is arranged in the phase/frequency control device PLL becomes synchronized to an adjacent transmission rate, for example PDH at 140 Mbit/s, the analysis of the incoming data frames according to the present invention makes it possible to identify and record the fact that the preselected transmission protocol is not being used and/or has not been identified. If, for example, the preselected transmission protocol is not identified, termination of the connection can be initiated automatically.

Automatic operation

When using the circuit arrangement illustrated in Figure 1 in the automatic operating mode, the clock signal ts which is produced by the phase/frequency control device PLL should be synchronized without any operator action to the digital data stream arriving at the data input ET, allowing subsequent "3D data regeneration" of the digital data stream ds. For this purpose, all the transmission protocols to be expected are stored in the table tab arranged in the memory MEM, together with the associated protocol-specific protocol identification information pid1...n and the associated control device control information PLL_WORD1...n for setting the phase/frequency control device PLL to the data transmission rate to be expected. When the automatic operating mode is activated, this causes the control

unit STRG to transmit the protocol identification information PID1...n and control device control information PLL_WORD1...n arranged in the table tab of the memory MEM step-by-step in the described manner and cyclically to the register unit REG and, respectively, to the memory register MR, until the comparator unit COMP identifies a defined transmission protocol stored in the table tab, and signals this to the control unit STRG. When a transmission protocol stored in the memory MEM is identified, the cyclic processing of the table tab arranged in the memory MEM is ended. If the currently selected transmission protocol is not identified, the described, successive run through the stored protocol identification information PID1...n and control device control information PLL_WORD1...n is carried out once again, after a predefined, protocol-specific delay.

The automatic protocol search sequence can be enabled only by an operator action. According to a further advantageous embodiment, selective enabling can be carried out by selection of the transmission protocols stored in the table tab via an appropriate identifier in the respective table entries te1...n.

In order to further improve the synchronization monitoring, the current state of the phase/frequency control device PLL can be detected with the aid of a generally known lock detector (not illustrated) which is also arranged in the phase/frequency control device PLL, and can be signaled to the control unit STRG.

The control/monitoring interface SS which is connected to the control unit STRG allows the table entries te1...n which are stored in the memory MEM to be processed and updated and, in addition to the monitoring of the respectively transmitted transmission protocols, allows the enabling of specific transmission protocols to be controlled. The control/monitoring interface SS also makes it possible to switch between the described manual or automatic operating modes. The control/monitoring interface SS can, for example, be connected to a higher-level network administration unit or network management unit so that, for example, it is possible for a network operator to monitor and to control the data transmission rate of the digital data stream ds arriving at the phase/frequency control device PLL.

The linking, according to the present invention, of the presetting of the data transmission rate to be expected to the phase/frequency control device PLL (which is generally known to those skilled in the art) and the checking of the transmission protocol used for transmitting the digital data stream by partial evaluation of the overhead information contained in the individual data frames avoids false synchronization of the clock signal to side lines, harmonics and subharmonics of the data transmission rate. The method according to the present invention also makes it possible to distinguish reliably between data transmission rates which are separated only slightly, by evaluation of the various overhead information items.

Although the present invention has been described with reference to specific embodiments, those of skill in the art will recognize that changes may be made thereto without departing from the spirit and scope of the invention as set forth in the hereafter appended claims.

ABSTRACT OF THE DISCLOSURE

A method and system for automatically producing clock signals for sampling data signals at different data rates via a phase locked loop, wherein in a synchronization process by means of the phase locked loop, a data signal is sampled successively using a clock signal at different frequencies, which are associated with different transmission protocols, and is checked for the presence of protocol identification information associated with the selected clock signal, until protocol identification information is detected such that the frequency resolution of the phase locked loop is advantageously increased, and the synchronization of the clock signal to the data signal is ~~thus~~ improved.

In the Claims:

On page 15, cancel line 1 and substitute the following left-hand justified heading therefor:

CLAIMS

Please cancel claims 1-14, without prejudice, and substitute the following claims therefor:

15. A method for automatically producing clock signals for sampling data signals at different data rates via a phase locked loop, the method comprising the steps of:

sampling, during a synchronization process, the data signal successively using a clock signal at different frequencies which are associated with different transmission protocols; and

checking the data signal, during the synchronization process, for the presence of protocol identification information associated with the selected clock signal until the protocol identification information is detected.

16. A method for automatically producing clock signals for sampling data signals at different data rates via a phase locked loop as claimed in claim 15, wherein the protocol identification information is included in an overhead of a data frame.

17. A method for automatically producing clock signals for sampling data signals at different data rates via a phase locked loop as claimed in claim 15, wherein the protocol identification information represents a pause signal.

18. A method for automatically producing clock signals for sampling data signals at different data rates via a phase locked loop as claimed in claim 16, the method further comprising the step of:

processing, once the protocol identification information has been detected, at least some of respective overhead information.

19. An apparatus for automatically producing clock signals for sampling data signals, which are transmitted with the aid of transmission protocols, at different data rates, the data signals having at least one binary protocol identification information item which uniquely identifies the transmission protocol, the apparatus comprising:

a phase locked loop for synchronization of the clock signal to the digital data signal passed to a phase/frequency control device;

at least one controllable frequency divider device arranged in a feedback path of the phase/frequency control device;

a sampling device for sampling the data signal with the aid of the clock signal;

a control unit for setting the clock signal to a frequency which corresponds to a transmission protocol; and

a protocol detector in which the control unit is arranged, the protocol detector storing at least a portion of the sampled data signal and investigating the sample data signal for the protocol identification information and transmitting an investigation result to the control unit which, if there is no protocol identification information, selects further defined frequencies for the clock signal until the protocol identification information is identified in the sampled data signal.

20. An apparatus for automatically producing clock signals for sampling data signals as claimed in claim 19, further comprising:

a memory connected to the control unit, the memory arranged in the protocol detector for storing at least one binary protocol identification information item and at least one control device control information item associated with the respective protocol identification information item and controlling the phase locked loop on a protocol-specific basis, wherein the control unit forms at least one control signal from the at least one control device control information item, with the at least one control signal being transmitted to the phase locked loop; and

a detector connected to the control unit and arranged in the protocol detector for detecting the stored protocol identification information which is associated with the at least one control device control information item in the sampled data signal, wherein the detector produces a control signal representing a detection result which is transmitted to the control unit, and wherein the control unit is designed such that at least one control signal, representing a frequency divider control information

item, is formed from the at least one stored control device control information item and is transmitted to the at least one frequency divider device.

21. An apparatus for automatically producing clock signals for sampling data signals as claimed in claim 20, wherein the control unit is designed such that, if a number of protocol identification information items are stored in the memory, the control device control information items associated with the number of protocol identification information items are transmitted successively to the phase locked loop, and the respectively associated protocol identification information items are detected successively in the sampled data stream, with the control device control information items being transmitted successively as a function of the detection result.

22. An apparatus for automatically producing clock signals for sampling data signals as claimed in claim 20, wherein the detector further comprises:

a shift register to which the sample data signal, the data signal and the clock signal are passed;

a comparator connected to both the shift register and the control unit; and

a memory register connected to both the comparator and the control unit for temporary storage of protocol identification information;

wherein the comparator is designed such that the protocol identification information stored in the memory register is compared with the data signal read to the shift register and a comparison result is transmitted to the control unit with the aid of the control signal.

23. An apparatus for automatically producing clock signals for sampling data signals as claimed in claim 20, wherein different protocol identification information items and overhead control information items associated therewith are stored in the memory, the sample data signal is supplied to an overhead processing unit which is connected to the control unit for processing protocol-specific

overhead information included in the data signal, and the overhead processing unit and the control unit are designed such that the overhead information is processed as a function of the at least one overhead control information item associated with the detected transmission protocol.

24. An apparatus for automatically producing clock signals for sampling data signals as claimed in claim 20, further comprising:

a control/monitoring interface to which the control unit is connected, via which the information stored in the memory can be updated and detection results can be transmitted to a higher-level communications unit.

25. An apparatus for automatically producing clock signals for sampling data signals as claimed in claim 20, wherein a number of voltage controlled oscillators can be selected as a function of the control device control information.

26. An apparatus for automatically producing clock signals for sampling data signals as claimed in claim 20, further comprising:

a frequency window discriminator provided in the phase locked loop which defines a frequency of the clock signal as a function of the control device control information and is set by the control unit.

27. An apparatus for automatically producing clock signals for sampling data signals as claimed in claim 19, further comprising:

a loop filter provided in the phase locked loop which is set by the control unit.

28. An apparatus for automatically producing clock signals for sampling data signals as claimed in claim 15, wherein the transmission protocol is selected from the group consisting of STM-1, STM-4, STM-16, fiber channel and Gigabit-Ethernet protocols.

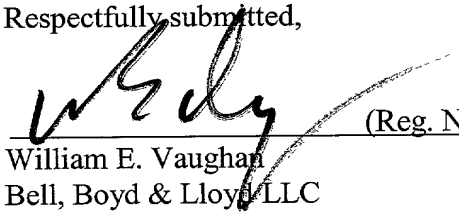
REMARKS

The present amendment makes editorial changes and corrects typographical errors in the specification, which includes the Abstract, in order to conform the specification to the requirements of United States Patent Practice. No new matter is added thereby. Attached hereto is a marked-up version of the changes made to the specification by the present amendment. The attached page is captioned "**Version With Markings To Show Changes Made**".

In addition, the present amendment cancels original claims 1-14 in favor of new claims 15-28. Claims 15-28 have been presented solely because the revisions by crossing out and underlining which would have been necessary in claims 1-14 in order to present those claims in accordance with preferred United States Patent Practice would have been too extensive, and thus would have been too burdensome. The present amendment is intended for clarification purposes only and not for substantial reasons related to patentability pursuant to 35 U.S.C. §§103, 102, 103 or 112. Indeed, the cancellation of claims 1-14 does not constitute an intent on the part of the Applicants to surrender any of the subject matter of claims 1-14.

Early consideration on the merits is respectfully requested.

Respectfully submitted,



(Reg. No. 39,056)

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Attorneys for Applicant

~~Description~~

SPECIFICATION

TITLE OF THE INVENTION

METHOD AND APPARATUS FOR AUTOMATICALLY PRODUCING CLOCK SIGNALS FOR SAMPLING DATA SIGNALS AT DIFFERENT DATA RATES VIA A PHASE LOCKED LOOP

~~Method and arrangement for automatically producing clock signals for sampling data signals at different data rates by means of a phase locked loop~~

The high level of transparency of optical networks with regard to data transmission rates and the use of different transmission methods and transmission protocols for the transmission of digital information (for example, the Synchronous Digital Hierarchy SDH, Gigabit-Ethernet, Fiber Channel) requires future devices for data regeneration and for reproduction of the amplitude, flank and clock of a transmitted digital data signal or data stream - also referred to as "3R data regeneration".

Apparatuses for producing a clock signal from a digital data stream or from a data signal stream are known. Phase/frequency control loops or phase locked loops are frequently used for clock recovery and include, for example, ~~comprise~~ a phase discriminator, a frequency discriminator, a loop filter, voltage controlled oscillators (also referred to as VCOs) and variable digital frequency dividers. The function of phase locked loops for clock recovery from a digital data stream and for sampling of the digital data stream to be regenerated ~~by means of~~ via a sampling flipflop are sufficiently well known to those skilled in the art, ~~so~~ such that their method of operation will not be described in ~~any more~~ further detail.

Various methods for determining the data transmission rate of the digital data stream are used to preset the phase locked loop. All the methods used, in particular, in wide area networks or WAN communications networks are based on more or less exactly determining the statistically distributed flank changes in the data stream within a defined observation time period. Conclusions can be drawn on

the actual data transmission rate from the number of flank changes identified. These methods are also referred to as flank density analyses. Apart from the described flank density analysis, period duration measurements of individual bits are also used for low transmission rates.

By way of example, Laid-Open Specification DE 197 04 299 A1 describes an apparatus for producing a clock signal from a data signal, and a bit rate identification device for determining the bit rate of the incoming data signal. The apparatus ~~comprises~~ includes a phase/frequency control device and a frequency divider device which is arranged in the feedback part of the phase/frequency control device and can be switched ~~by means of~~ via a data word. The switchable frequency divider device is connected to the bit rate identification device, to which the digital data stream and at least one reference frequency signal can be supplied. The bit rate identification device provides a bit-rate-dependent data word as a function of the applied reference frequency signal and the digital data stream passed to it~~,~~. ~~and this~~ This is then supplied to the frequency divider device arranged in the phase/frequency control device. The described apparatus for producing a clock signal from a digital data signal or data stream has the disadvantage that the resolution of the identification circuit is highly limited~~,~~; that is, ~~to say~~ digital data stream transmission rates which differ by less than a factor of 4 cannot be distinguished reliably in this way. A further disadvantage is the risk of false synchronization to side lines in the frequency spectrum during the transmission of certain data contents; for example, when transmitting AIS information in SDH signals (Synchronous Digital Hierarchy).

The present invention is, therefore, directed toward ~~based on the object of~~ improving the production of a clock signal from a transmitted digital data signal during a synchronization process and, in particular, the synchronization of the clock signal to the incoming digital data signal. ~~The object is achieved by a method and by an arrangement based on a method and an arrangement according to the features of the precharacterizing clause of patent claims 1 and 5, by virtue of the characterizing features in these claims.~~

SUMMARY OF THE INVENTION

The method according to the present invention provides for automatic production of clock signals for sampling data signals at different data rates ~~by means of~~ via a phase locked loop. ~~The~~ A major aspect of the method according to the present invention is that, during a synchronization process, the data signal is sampled successively using a clock signal at different frequencies, which are associated with different transmission protocols, and is checked for the presence of protocol identification information associated with the selected clock signal, until protocol identification information is detected.

~~The~~ A major advantage of the method according to the present invention is that the link between the detection of the transmission rate of the transmitted digital data signal and the detection of the transmission protocol that is matched to the frequency of the digital data signal or of the clock signal that is produced avoids false synchronization of the clock signal that is produced to side lines, harmonics and subharmonics of the transmission frequency or transmission rate of the data signal. The method according to the present invention also makes it possible to distinguish reliably between transmission rates that are arranged adjacent in the frequency domain; for example, distinguishing between "Gigabit-Ethernet" at a transmission rate of 1.25 Gbit/s and "Fiber Channel" at a transmission rate of 1.064 Gbit/s. A further advantage of the method according to the present invention is that it allows the transmission rate to be set automatically to "3R data regeneration" for frame-oriented transmission methods, and automatic identification of the respective transmission protocol. In future optical communication networks, the method according to the present invention will allow not only pure wavelength conversion ~~by means of~~ via flexible "3R data regeneration", but also analysis of the respectively transmitted digital data signals or data streams; for example, for the preprocessing of statistics, in order to provide network planning, or for volume-dependent billing.

Additional features and advantages of the present invention are described in, and will be apparent from, the following Detailed Description of the Invention and the Figures.

~~Further advantageous refinements of the method according to the invention, and an arrangement for automatically producing clock signals, can be found in the further claims.~~

~~The method according to the invention will be explained in more detail in the following text with reference to the drawings, in which:~~

BRIEF DESCRIPTION OF THE FIGURES

Figure 1 shows a circuit arrangement for producing a clock signal, according to the present invention, from a transmitted digital data stream~~, and~~.

Figure 2 shows an example of a tabular representation of the binary information which is required to carry out the method according to the present invention and is stored in a memory in the circuit arrangement.

DETAILED DESCRIPTION OF THE INVENTION

Figure 1 uses a block diagram to show an exemplary embodiment of a circuit arrangement for producing a clock signal ts from a digital data signal or data stream ds passed to it. The circuit arrangement illustrated in Figure 1 is subdivided into two functional circuit units PLL, RD, which are each represented by a rectangle with a dashed-dotted outline. The first functional circuit unit ~~comprises~~ includes a phase/frequency control device (PLL), which is generally known to those skilled in the art and is also referred to as a phase locked loop or PLL circuit~~, and the~~. The second circuit unit ~~comprises~~ includes a frame identification RD, which is connected to the phase/frequency control device (PLL) and is also referred to in the following text as frame detector.

A digital data stream ds transmitted with the aid of a transmission protocol is passed to one input ET of the phase/frequency control device PLL and is passed on to an input EF of a sampling flipflop AFF. In the exemplary embodiment, it is assumed that the data stream ds is transmitted in accordance with the Synchronous Digital Hierarchy - SDH. The Synchronous Digital Hierarchy is based on

synchronous transmission of user information using synchronous transport modules (also referred to as STM) with a standard structure. The basic transport module is the STM-1 frame, with a data transmission rate of 155 Mbit/s. Each STM-1 frame ~~comprises~~ includes a matrix of 9 rows each having 270 data octets. The frame has a repetition frequency of 125 µs, and the transmission is carried out at a bit rate of 155.520 Mbit/s. The STM-1 frame is inserted into a payload and an overhead, with the first 9 octets in all 9 rows containing the overhead, and the remaining columns containing the payload. The overhead contains information which is required to operate SDH systems, and these are also referred to as section overheads (SOH) and are transported in the SOH areas of the overhead. The SOH areas contain, for example, the A1 and A2 bytes, which are known to those skilled in the art, and which each represent frame identification information.

The data input ET of the phase/frequency control device PLL is at the same time connected to a first input EP of a discriminator unit DE. A reference signal f_{Ref} at a reference frequency is passed to a second input EF of the discriminator unit DE. The discriminator unit DE is functionally subdivided into two components, a phase discriminator PD and a frequency window discriminator FD, each indicated by a rectangle with a dashed outline.

The discriminator unit DE is connected via an output AP to an input EL of a loop filter LF, which is, in turn, connected via an output AL to an input EV of a voltage controlled oscillator VCO. A first and a second variable digital frequency divider T1,T2 is each connected via an input ET to an output AV of the voltage controlled oscillator VCO. The first digital frequency divider T1 is connected to a clock input CLK of the phase discriminator PD, and the second digital frequency divider T2 is connected to a divider input ETF of the frequency window discriminator FD, in each case via an output AT. The described discriminator unit DE, ~~comprising~~ including a phase window discriminator PD and a frequency window discriminator FD, as well as the loop filter LF, the voltage controlled oscillator VCO and the two variable digital frequency dividers T1, T2 are functional components of a generally known phase locked loop, whose function for recovery

of the clock from the data stream ds passed to it in addition to the sampling of the data stream ds to be regenerated in conjunction with the sampling flipflop AFF are sufficiently well known to those skilled in the art, and will not be described in any more detail in the following text.

The phase/frequency control device PLL has a clock output CA which is connected to the output AT of the first frequency divider T1, and to which the clock signal ts which is produced is passed. The output AT of the first frequency divider T1 is, in turn, connected to a clock input CLK of the sampling flipflop AFF. The sampling flipflop AFF is connected via an output AF to a data output AT of the phase/frequency control device PLL, to which the data stream cds, regenerated ~~by means of~~ via the sampling flipflop AFF, is passed. Furthermore, the output AF of the sampling flipflop AFF is connected to an input ES of a shift register SR arranged in the frame identification unit RD. The shift register SR has a clock input CLK, which is connected to the output AT of the first frequency divider T1.

Furthermore, a memory MEM is arranged in the frame identification unit RD and is connected via a connecting line to a control unit STRG arranged in the frame identification unit RD. A table tab, illustrated in Figure 2, is stored in the memory MEM. The illustrated table tab has a number of table entries te1...n, with each table entry te1...n having a respectively associated, defined transmission protocol. Each table entry te1...n is used to store protocol identification information PID1...n which uniquely identifies the respectively defined transmission protocol (for example, the frame identification information contained in the overhead information, in this case the A1 and A2 bytes) control loop control information PLL_WORD1...n for setting the phase/frequency control device PLL to the transmission rate to be expected for the data stream ds, and further overhead control information CNT_WD1...n for optional protocol-specific evaluation and processing of the overhead information arranged in the respective data packets or data frames of the data stream ds, cds. The overhead control information CNT_WD1...n can be used to evaluate, and if necessary to recalculate, for example, the B1 byte contained

in the overhead information in a data stream transmitter using the SDH transmission method.

The control unit STRG is connected via a data bus DB having a number of data lines to a memory register MR, which is arranged in the frame identification unit RD and to which protocol identification information PID1...n which is stored in the memory MEM can ~~in each case~~ be transmitted~~,~~ and ~~can be~~ stored therein; indicated by a rectangle with a dashed outline. The shift register SR and the memory register MR are connected via respective outputs AS, AM and a respective number of data lines DL1...n to corresponding inputs EC of a comparator unit COMP. The comparator COMP has comparison ~~means~~ capabilities which are used to compare the binary information or data words applied to the inputs EC, and the comparison result is transmitted in the form of a data signal int via an output AC and a signaling line SCS to an input ES of the control unit STRG.

The data bus DB is also used to connect the control unit STRG to a register unit REG, which is connected via first outputs A1 and via first control lines SL1 to a control input S of the frequency window discriminator FD, via second outputs A2 and via second control lines SL2 to corresponding control inputs S of the second controllable frequency divider T2, via third outputs A3 and third control lines SL3 to corresponding inputs S of the first controllable frequency divider T1, and via fourth outputs A4 and fourth control lines SL4 to corresponding inputs S of the voltage controlled oscillator VCO. The register unit REG has one or more memory registers (Figure 1 shows only one memory register, in the form of a rectangle with a dashed outline) in each of which the control device control information PLL_WORD1...n stored in the memory MEM, or control words or binary information derived from such control information, can be stored, ~~by means of~~ via which the circuitry components, in this case FD, PD, LF, VCO, T1 and T2, arranged in the phase/frequency control device PLL can be controlled. Alternatively, analog signals can be derived from the control words stored in the register REG, and can be supplied to the circuitry components.

The frame identification unit RD also has a control/monitoring interface SS, which is connected to the control unit STRG via a connecting line.

The method, which can be implemented ~~by means of~~ via the circuit arrangement illustrated in Figure 1, for producing a clock signal ts from the digital data stream ds transmitted with the aid of a transmission protocol optionally allows both the manual and automatic selection of a transmission protocol, and corresponding presetting of a data transmission rate matched to the selected transmission protocol. The method for producing the clock signal ts on the basis of manual selection, also referred to as a manual operating mode, and on the basis of automatic selection, also referred to as an automatic operating mode - of the transmission protocol and of the associated data transmission rate is explained in more detail in the following text with reference to the circuit arrangement illustrated in Figure 1. For the further exemplary embodiment, it is assumed that the digital data stream ds is transmitted with the aid of a frame-oriented transmission protocol, in this case STM-1, to the input ET of the phase/frequency control device (PLL) and is passed on to the data input EF of the sampling flipflop AFF.

Manual operating mode

During manual operation of the circuit arrangement, the transmission protocol with which the digital data stream ds is transmitted to the data input EF of the sampling flipflop AFF is known. On the basis of the knowledge of the transmission protocol, the control unit STRG arranged in the frame identification unit RD selects the first table entry te1 that is associated with the STM-1 transmission protocol in the table tab and reads the corresponding control loop control information, in this case PLL_WORD1, from the memory MEM, and transmits this via the data bus DB to the corresponding register or registers in the register unit REG. Alternatively, further control information can be derived from the transmitted control loop control information PLL_WORD, and can be stored in the corresponding register in the register unit REG. According to a further ~~refinement variant~~ embodiment (not illustrated) a number of control words or control device control information items associated with the STM-1 transmission

protocol ~~can~~ also can be stored in the respective table entries te1...n in the table tab (not illustrated in Figure 2), which are transmitted via the data bus DB to corresponding registers in the register unit REG. The transmission of the control loop control information PLL_WORD1...n stored in the memory MEM allows the circuitry components VCO, T1, T2, FD, PD, LF to be preset to the corresponding data transmission rate of the incoming digital data stream ds, in this case 155 Mbit/s. Furthermore, the control unit STRG reads the protocol identification information, in this case PID1, associated with the selected transmission protocol, in this case STM-1, from the corresponding table entry te1 in the table tab, and transmits this via the data bus DB to the memory register MR, in which it is temporarily stored. In this exemplary embodiment, the frame identification word which is specific for the STM-1 transmission protocol and ~~comprises~~ includes the last A1 and the first A2 byte of the overhead information is transmitted as the protocol identification information PID1 to the memory register REG.

As already explained, the phase locked loop which is arranged in the phase/frequency control device PLL is matched to the data transmission rate of the incoming digital data stream ds ~~by means of~~ via the control loop control information PLL_WORD1 stored in the register unit REG. By way of example, the transmission of appropriate control information si2,3 via the control lines SL2 and SL3 sets the controllable frequency dividers T1, T2 such that the frequency of the signal delivered from the voltage controlled oscillator VCO is divided as appropriate for matching of the optimum operating point of the phase discriminator PD and of the frequency window discriminator FD. Additional control information, in this case si4, transmitted via the fourth control line SL4 is used to provide any possibly required presetting or switching of the voltage controlled oscillator VCO. According to one alternative ~~refinement variant~~ embodiment of the circuit arrangement, a number of voltage controlled oscillators VCO can be arranged in the phase/frequency control device PLL, in which case one voltage controlled oscillator VCO, which is matched to the data transmission rate of the incoming digital data

stream ds, ~~can~~ in each can case be selected with the aid of the fourth control signal si4.

According to a further ~~refinement variant~~ embodiment of the circuit arrangement, which is not illustrated in Figure 1, the loop filter LF arranged in the phase/frequency control device PLL is likewise controlled as a function of the control loop control information PLL_WORD1...n stored in the register unit REG.

The digital data stream cds sampled with the aid of the recovered clock signal ts is read to the shift register SR, that is to say the shift register SR contains the data bits read with the aid of the recovered clock ts. Alternatively, the data stream ds which is applied to the input ET but is not sampled ~~can~~ also can be read to the shift register SR, which is clocked by the clock signal ts, via a connecting line, indicated by a dashed connecting line in Figure 1.

The bit sequence read to the shift register SR is permanently compared by the comparator unit COMP with the protocol identification information, in this case pid1, temporarily stored in the memory register MR. If the comparator unit COMP finds a match or a partial match between the digital bit sequence that is read and the protocol identification information pid1, a corresponding control signal int is generated in the comparator unit COMP, and is transmitted via the control line SCS to the control unit STRG. The transmission of the control information int to the control unit STRG indicates the identification of the selected transmission protocol, in this case STM1, and the setting of the associated data transmission rate for the phase/frequency control device PLL.

In order to improve the synchronization of the clock signal ts that is produced to the incoming digital data stream ds, according to a further ~~refinement variant~~ embodiment that is not illustrated, the control unit STRG checks whether the protocol identification information, in this case pid1, is identified more than once, for example three times, in a cycle time which is specific for the selected transmission protocol. If the transmission protocol being used ~~means that~~ resulting the frame sequence ~~is~~ being asynchronous, for example when using the Gigabit-

Ethernet transmission protocol, this ~~refinement variant~~ embodiment allows the pause pattern, ~~also referred to as the~~ or "Interframe Gap", to be analyzed.

When the selected or expected protocol identification information pid1 is identified in the sampled data stream cds, the start of data transmission can be recorded ~~by means of~~ via the control unit STRG. If there are no periodically produced data frames, for example when using the STM-1 transmission protocol, it is advantageously possible in conjunction with further parameters, for example loss of the signal (LOS) or optical level, to deduce that there is a fault or that this is the end of transmission. In the situation where the phase locked loop which is arranged in the phase/frequency control device PLL becomes synchronized to an adjacent transmission rate, for example PDH at 140 Mbit/s, the analysis of the incoming data frames according to the present invention makes it possible to identify and record the fact that the preselected transmission protocol is not being used and/or has not been identified. If, for example, the preselected transmission protocol is not identified, termination of the connection can be initiated automatically.

Automatic operation

When using the circuit arrangement illustrated in Figure 1 in the automatic operating mode, the clock signal ts which is produced by the phase/frequency control device PLL should be synchronized without any operator action to the digital data stream arriving at the data input ET, allowing subsequent "3D data regeneration" of the digital data stream ds. For this purpose, all the transmission protocols to be expected are stored in the table tab arranged in the memory MEM, together with the associated protocol-specific protocol identification information pid1...n and the associated control device control information PLL_WORD1...n for setting the phase/frequency control device PLL to the data transmission rate to be expected. When the automatic operating mode is activated, this causes the control unit STRG to transmit the protocol identification information PID1...n and control device control information PLL_WORD1...n arranged in the table tab of the memory MEM step-by-step in the described manner and cyclically to the register unit REG and, respectively, to the memory register MR, until the comparator unit

COMP identifies a defined transmission protocol stored in the table tab, and signals this to the control unit STRG. When a transmission protocol stored in the memory MEM is identified, the cyclic processing of the table tab arranged in the memory MEM is ended. If the currently selected transmission protocol is not identified, the described, successive run through the stored protocol identification information PID1...n and control device control information PLL_WORD1...n is carried out once again, after a predefined, protocol-specific delay.

The automatic protocol search sequence can ~~advantageously~~ be enabled only by an operator action. According to a further advantageous ~~refinement~~ embodiment, selective enabling can be carried out by selection of the transmission protocols stored in the table tab ~~by means of~~ via an appropriate identifier in the respective table entries te1...n.

In order to further improve the synchronization monitoring, the current state of the phase/frequency control device PLL can be detected with the aid of a generally known lock detector (not illustrated) which is also arranged in the phase/frequency control device PLL, and can be signaled to the control unit STRG.

The control/monitoring interface SS which is connected to the control unit STRG allows the table entries te1...n which are stored in the memory MEM to be processed and updated and, in addition to the monitoring of the respectively transmitted transmission protocols, allows the enabling of specific transmission protocols to be controlled. The control/monitoring interface SS also makes it possible to switch between the described manual or automatic operating modes. The control/monitoring interface SS can, for example, be connected to a higher-level network administration unit or network management unit so that, for example, it is possible for a network operator to monitor and to control the data transmission rate of the digital data stream ds arriving at the phase/frequency control device PLL.

The linking, according to the present invention, of the presetting of the data transmission rate to be expected to the phase/frequency control device PLL (which is generally known to those skilled in the art) and the checking of the transmission protocol used for transmitting the digital data stream by partial evaluation of the

overhead information contained in the individual data frames avoids false synchronization of the clock signal to side lines, harmonics and subharmonics of the data transmission rate. The method according to the present invention also makes it possible to distinguish reliably between data transmission rates which are separated only slightly, by evaluation of the various overhead information items.

Although the present invention has been described with reference to specific embodiments, those of skill in the art will recognize that changes may be made thereto without departing from the spirit and scope of the invention as set forth in the hereafter appended claims.

BOX PCT

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UNDER THE PATENT COOPERATION TREATY-CHAPTER II

SUBMISSION OF DRAWINGS

APPLICANT:	Fritz-Joerg Dauth	DOCKET NO.:	112740-321
SERIAL NO:		GROUP ART UNIT:	
FILED:		EXAMINER:	
INTERNATIONAL APPLICATION NO.		PCT/DE00/00641	
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INVENTION: METHOD AND APPARATUS FOR AUTOMATICALLY PRODUCING CLOCK SIGNALS FOR SAMPLING DATA SIGNALS AT DIFFERENT DATA RATES VIA A PHASE LOCKED LOOP

Assistant Commissioner for Patents,
Washington, D.C. 20231

Sir:

Applicant herewith submits two sheets (Figs. 1-2) of drawings for the above-referenced PCT application.

Respectfully submitted,

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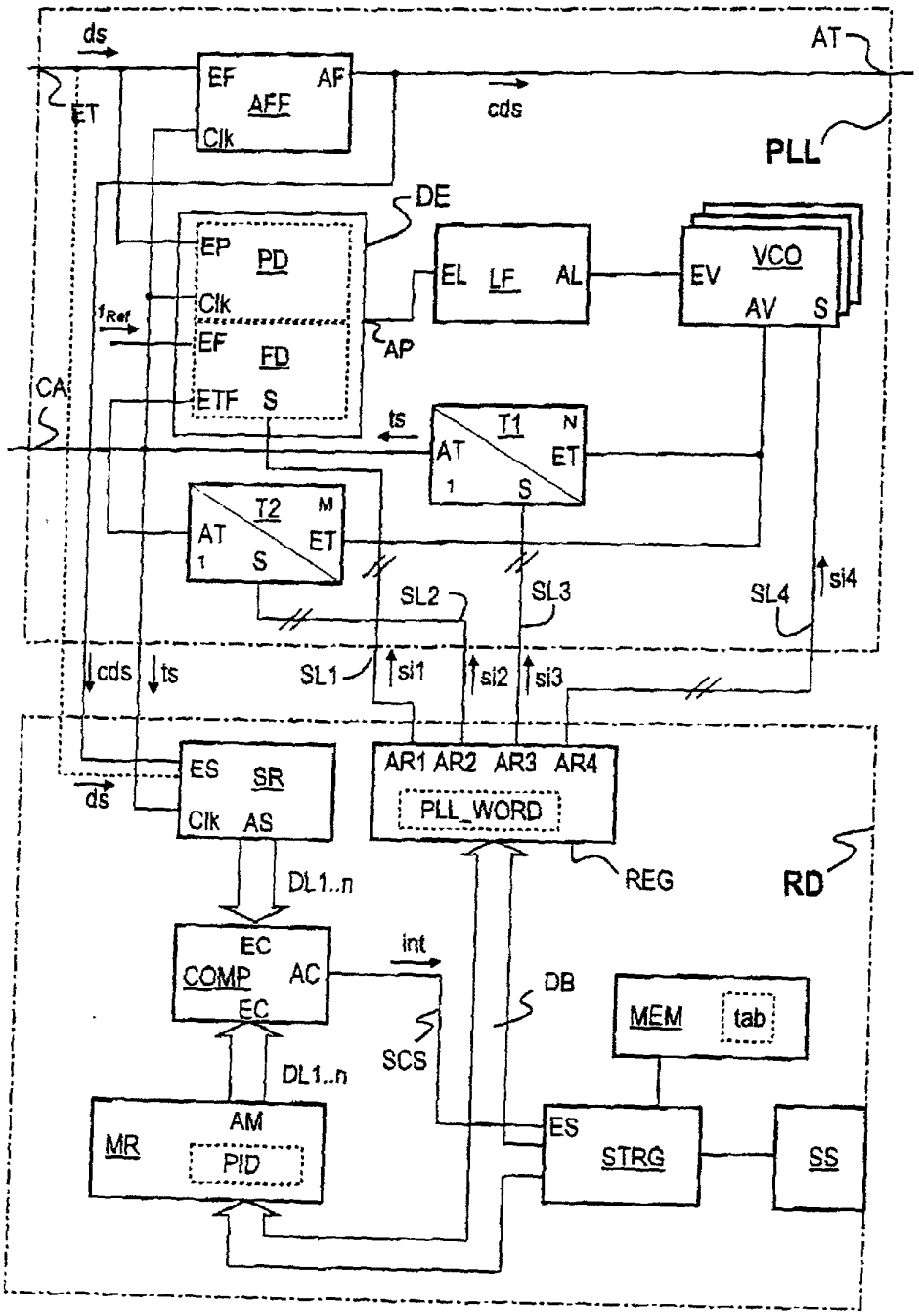
FIG 1


ds
AT
EF
AF
AFF
ET
Clk
cds
PLL
DE
EP
PD
EL
LF
AL
EV
VCO
AV
S
Clk
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CA
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T1
N
AT
ET
1
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T2
M
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ET
1
S
SL2
SL3
SL4
si4
cds
ts
SL1
si1
si2
si3
ES
SR
Clk
AS
AR1 AR2 AR3 AR4
PLL_WORD
REG
RD
DL1..n
EC
COMP
AC
EC
int
DB
MEM
tab
SCS
DL1..n
AM
MR
PID
ES
STRG
SS

FIG 2

tab

Data set No.	Transmission protocol	Protocol identification information	Control device control information	Overhead control information
te1	SDH (STM-1) (155 Mbit/s)	PID1 (e.g. A1 and A2 byte in the SOH of an SDH signal)	PLL_WORD1	CNT_WD1
te2	SDH (STM-4) (622 Mbit/s)	PID2 (e.g. A1 and A2 byte in the SOH of an SDH signal)	PLL_WORD2	CNT_WD2
te3	SDH (STM-16) (2.5 Gbit/s)	PID3 (e.g. A1 and A2 byte in the SOH of an SDH signal)	PLL_WORD3	CNT_WD3
te4	Gigabit-Ethernet (1.25 Gbit/s)	PID4 (Idle; Preamble; SFD-"Start Frame Delimiter")	PLL_WORD4	CNT_WD4
te n	.....	PIDn	PLL_WORDn	CNT_WDn

09/96670

Method and arrangement for automatically producing clock signals for sampling data signals at different data rates by means of a phase locked loop

The high level of transparency of optical networks with regard to data transmission rates and the use of different transmission methods and transmission protocols for the transmission of digital information - for example the Synchronous Digital Hierarchy SDH, Gigabit-Ethernet, Fiber Channel - requires future devices for data regeneration and for reproduction of the amplitude, flank and clock of a transmitted digital data signal or data stream - also referred to as "3R data regeneration".

Apparatuses for producing a clock signal from a digital data stream or from a data signal stream are known. Phase/frequency control loops or phase locked loops are frequently used for clock recovery and, for example, comprise a phase discriminator, a frequency discriminator, a loop filter, voltage controlled oscillators - also referred to as VCOs - and variable digital frequency dividers. The function of phase locked loops for clock recovery from a digital data stream and for sampling of the digital data stream to be regenerated by means of a sampling flipflop are sufficiently well known to those skilled in the art, so that their method of operation will not be described in any more detail.

Various methods for determining the data transmission rate of the digital data stream are used to preset the phase locked loop. All the methods used in particular in wide area networks or WAN communications networks are based on more or less exactly determining the statistically distributed flank changes in the data stream within a defined observation time

period. Conclusions can be drawn on the actual data transmission rate from the number of flank changes identified. These methods are also referred to as flank density analyses. Apart from the described flank density analysis, period duration measurements of individual bits are also used for low transmission rates.

By way of example, Laid-Open Specification DE 197 04 299 A1 describes an apparatus for producing a clock signal from a data signal, and a bit rate identification device for determining the bit rate of the incoming data signal. The apparatus comprises a phase/frequency control device and a frequency divider device which is arranged in the feedback part of the phase/frequency control device and can be switched by means of a data word. The switchable frequency divider device is connected to the bit rate identification device, to which the digital data stream and at least one reference frequency signal can be supplied. The bit rate identification device provides a bit-rate-dependent data word as a function of the applied reference frequency signal and the digital data stream passed to it, and this is then supplied to the frequency divider device arranged in the phase/frequency control device. The described apparatus for producing a clock signal from a digital data signal or data stream has the disadvantage that the resolution of the identification circuit is highly limited, that is to say digital data stream transmission rates which differ by less than a factor of 4 cannot be distinguished reliably in this way. A further disadvantage is the risk of false synchronization to side lines in the frequency spectrum during the transmission of certain data contents - for example when transmitting AIS information in SDH signals - Synchronous Digital Hierarchy.

The invention is based on the object of improving the

production of a clock signal from a transmitted digital data signal

during a synchronization process and, in particular, the synchronization of the clock signal to the incoming digital data signal. The object is achieved by a method and by an arrangement based on a method and an arrangement according to the features of the precharacterizing clause of patent claims 1 and 5, by virtue of the characterizing features in these claims.

The method according to the invention provides for automatic production of clock signals for sampling data signals at different data rates by means of a phase locked loop. The major aspect of the method according to the invention is that, during a synchronization process, the data signal is sampled successively using a clock signal at different frequencies, which are associated with different transmission protocols, and is checked for the presence of protocol identification information associated with the selected clock signal, until protocol identification information is detected.

The major advantage of the method according to the invention is that the link between the detection of the transmission rate of the transmitted digital data signal and the detection of the transmission protocol that is matched to the frequency of the digital data signal or of the clock signal that is produced avoids false synchronization of the clock signal that is produced to side lines, harmonics and subharmonics of the transmission frequency or transmission rate of the data signal. The method according to the invention also makes it possible to distinguish reliably between transmission rates that are arranged adjacent in the frequency domain - for example, distinguishing between "Gigabit-Ethernet" at a transmission rate of 1.25 Gbit/s and "Fiber Channel" at a transmission rate of 1.064 Gbit/s. A further advantage of the method according to the invention is that it allows the transmission rate to be set automatically to "3R data regeneration" for frame-oriented transmission methods,

and automatic

identification of the respective transmission protocol. In future optical communication networks, the method according to the invention will allow not only pure wavelength conversion by means of flexible "3R data regeneration", but also analysis of the respectively transmitted digital data signals or data streams - for example for the preprocessing of statistics, in order to provide network planning, or for volume-dependent billing.

Further advantageous refinements of the method according to the invention, and an arrangement for automatically producing clock signals, can be found in the further claims.

The method according to the invention will be explained in more detail in the following text with reference to the drawings, in which:

Figure 1 shows a circuit arrangement for producing a clock signal, according to the invention, from a transmitted digital data stream, and

Figure 2 shows an example of a tabular representation of the binary information which is required to carry out the method according to the invention and is stored in a memory in the circuit arrangement.

Figure 1 uses a block diagram to show an exemplary embodiment of a circuit arrangement for producing a clock signal ts from a digital data signal or data stream ds passed to it. The circuit arrangement illustrated in Figure 1 is subdivided into two functional circuit units PLL, RD, which are each represented by a rectangle with a dashed-dotted outline. The first functional circuit unit comprises a phase/frequency control device (PLL), which is generally known to those skilled in the art and is also

referred to as a phase locked loop or PLL circuit, and the second circuit unit comprises a frame identification RD, which is connected to the phase/frequency control device (PLL)

and is also referred to in the following text as frame detector.

A digital data stream ds transmitted with the aid of a transmission protocol is passed to one input ET of the phase/frequency control device PLL and is passed on to an input EF of a sampling flipflop AFF. In the exemplary embodiment, it is assumed that the data stream ds is transmitted in accordance with the Synchronous Digital Hierarchy - SDH. The Synchronous Digital Hierarchy is based on synchronous transmission of user information using synchronous transport modules - also referred to as STM - with a standard structure. The basic transport module is the STM-1 frame, with a data transmission rate of 155 Mbit/s. Each STM-1 frame comprises a matrix of 9 rows each having 270 data octets. The frame has a repetition frequency of 125 µs, and the transmission is carried out at a bit rate of 155.520 Mbit/s. The STM-1 frame is inserted into a payload and an overhead, with the first 9 octets in all 9 rows containing the overhead, and the remaining columns containing the payload. The overhead contains information which is required to operate SDH systems, and these are also referred to as section overheads - SOH - and are transported in the SOH areas of the overhead. The SOH areas contain, for example, the A1 and A2 bytes, which are known to those skilled in the art, and which each represent frame identification information.

The data input ET of the phase/frequency control device PLL is at the same time connected to a first input EP of a discriminator unit DE. A reference signal f_{Ref} at a reference frequency is passed to a second input EF of the discriminator unit DE. The discriminator unit DE is functionally subdivided into two components, a phase discriminator PD and a frequency window discriminator FD - each indicated by a rectangle with a dashed outline.

The discriminator unit DE is connected via an output AP to an input EL of a loop filter LF, which is in turn connected via an output AL to an input EV of a voltage controlled oscillator VCO. A first and a second variable digital frequency divider T1,T2 is each connected via an input ET to an output AV of the voltage controlled oscillator VCO. The first digital frequency divider T1 is connected to a clock input CLK of the phase discriminator PD, and the second digital frequency divider T2 is connected to a divider input ETF of the frequency window discriminator FD, in each case via an output AT. The described discriminator unit DE, comprising a phase window discriminator PD and a frequency window discriminator FD, as well as the loop filter LF, the voltage controlled oscillator VCO and the two variable digital frequency dividers T1, T2 are functional components of a generally known phase locked loop, whose function for recovery of the clock from the data stream ds passed to it in addition to the sampling of the data stream ds to be regenerated in conjunction with the sampling flipflop AFF are sufficiently well known to those skilled in the art, and will not be described in any more detail in the following text.

The phase/frequency control device PLL has a clock output CA which is connected to the output AT of the first frequency divider T1, and to which the clock signal ts which is produced is passed. The output AT of the first frequency divider T1 is in turn connected to a clock input CLK of the sampling flipflop AFF. The sampling flipflop AFF is connected via an output AF to a data output AT of the phase/frequency control device PLL, to which the data stream cds, regenerated by means of the sampling flipflop AFF, is passed. Furthermore, the output AF of the sampling flipflop AFF is connected to an input ES of a shift register SR arranged in the frame identification unit RD. The shift register SR has a clock input CLK, which is connected to the output AT of the first frequency divider T1.

Furthermore, a memory MEM is arranged in the frame identification unit RD and is connected via a connecting line to a control unit STRG arranged in the frame identification unit RD. A table tab, illustrated in Figure 2, is stored in the memory MEM. The illustrated table tab has a number of table entries te1...n, with each table entry te1...n having a respectively associated, defined transmission protocol. Each table entry te1...n is used to store protocol identification information PID1...n which uniquely identifies the respectively defined transmission protocol - for example the frame identification information contained in the overhead information, in this case the A1 and A2 bytes - control loop control information PLL_WORD1...n for setting the phase/frequency control device PLL to the transmission rate to be expected for the data stream ds, and further overhead control information CNT_WD1...n for optional protocol-specific evaluation and processing of the overhead information arranged in the respective data packets or data frames of the data stream ds, cds. The overhead control information CNT_WD1...n can be used to evaluate, and if necessary to recalculate, for example the B1 byte contained in the overhead information in a data stream transmitter using the SDH transmission method.

The control unit STRG is connected via a data bus DB having a number of data lines to a memory register MR, which is arranged in the frame identification unit RD and to which protocol identification information PID1...n which is stored in the memory MEM can in each case be transmitted, and can be stored therein - indicated by a rectangle with a dashed outline. The shift register SR and the memory register MR are connected via respective outputs AS, AM and a respective number of data lines DL1...n to corresponding inputs EC of a comparator unit COMP. The comparator COMP has comparison

means which are used to compare the binary information or data words applied to the inputs EC, and the comparison result is transmitted in the form of a data signal int via an output AC and a signaling line SCS to an input ES of the control unit STRG.

The data bus DB is also used to connect the control unit STRG to a register unit REG, which is connected via first outputs A1 and via first control lines SL1 to a control input S of the frequency window discriminator FD, via second outputs A2 and via second control lines SL2 to corresponding control inputs S of the second controllable frequency divider T2, via third outputs A3 and third control lines SL3 to corresponding inputs S of the first controllable frequency divider T1, and via fourth outputs A4 and fourth control lines SL4 to corresponding inputs S of the voltage controlled oscillator VCO. The register unit REG has one or more memory registers - Figure 1 shows only one memory register, in the form of a rectangle with a dashed outline - in each of which the control device control information PLL_WORD1...n stored in the memory MEM, or control words or binary information derived from such control information, can be stored, by means of which the circuitry components - in this case FD, PD, LF, VCO, T1 and T2 - arranged in the phase/frequency control device PLL can be controlled. Alternatively, analog signals can be derived from the control words stored in the register REG, and can be supplied to the circuitry components.

The frame identification unit RD also has a control/monitoring interface SS, which is connected to the control unit STRG via a connecting line.

The method, which can be implemented by means of the circuit arrangement illustrated in Figure 1, for producing a clock signal ts from the digital data stream ds transmitted with the aid of a transmission

protocol optionally allows both the

manual and automatic selection of a transmission protocol, and corresponding presetting of a data transmission rate matched to the selected transmission protocol. The method for producing the clock signal ts on the basis of manual selection - also referred to as a manual operating mode - and on the basis of automatic selection - also referred to as an automatic operating mode - of the transmission protocol and of the associated data transmission rate is explained in more detail in the following text with reference to the circuit arrangement illustrated in Figure 1. For the further exemplary embodiment, it is assumed that the digital data stream ds is transmitted with the aid of a frame-oriented transmission protocol - in this case STM-1 - to the input ET of the phase/frequency control device (PLL) and is passed on to the data input EF of the sampling flipflop AFF.

Manual operating mode

During manual operation of the circuit arrangement, the transmission protocol with which the digital data stream ds is transmitted to the data input EF of the sampling flipflop AFF is known. On the basis of the knowledge of the transmission protocol, the control unit STRG arranged in the frame identification unit RD selects the first table entry te1 that is associated with the STM-1 transmission protocol in the table tab and reads the corresponding control loop control information - in this case PLL_WORD1 - from the memory MEM, and transmits this via the data bus DB to the corresponding register or registers in the register unit REG. Alternatively, further control information can be derived from the transmitted control loop control information PLL_WORD, and can be stored in the corresponding register in the register unit REG. According to a further refinement variant - not illustrated - a number of control words or control device control information items associated with the

STM-1 transmission protocol can also be stored in the respective table entries te1...n in the table tab - not illustrated in Figure 2 -, which are

transmitted via the data bus DB to corresponding registers in the register unit REG. The transmission of the control loop control information PLL_WORD1...n stored in the memory MEM allows the circuitry components VCO, T1, T2, FD, PD, LF to be preset to the corresponding data transmission rate of the incoming digital data stream ds - in this case 155 Mbit/s. Furthermore, the control unit STRG reads the protocol identification information - in this case PID1 - associated with the selected transmission protocol - in this case STM-1 - from the corresponding table entry te1 in the table tab, and transmits this via the data bus DB to the memory register MR, in which it is temporarily stored. In this exemplary embodiment, the frame identification word which is specific for the STM-1 transmission protocol and comprises the last A1 and the first A2 byte of the overhead information is transmitted as the protocol identification information PID1 to the memory register REG.

As already explained, the phase locked loop which is arranged in the phase/frequency control device PLL is matched to the data transmission rate of the incoming digital data stream ds by means of the control loop control information PLL_WORD1 stored in the register unit REG. By way of example, the transmission of appropriate control information si2,3 via the control lines SL2 and SL3 sets the controllable frequency dividers T1, T2 such that the frequency of the signal delivered from the voltage controlled oscillator VCO is divided as appropriate for matching of the optimum operating point of the phase discriminator PD and of the frequency window discriminator FD. Additional control information - in this case si4 - transmitted via the fourth control line SL4 is used to provide any possibly required presetting or switching of the voltage controlled oscillator VCO. According to one alternative refinement variant of the circuit arrangement, a number of voltage controlled oscillators

VCO can be arranged in the phase/frequency control device PLL, in which case

one voltage controlled oscillator VCO, which is matched to the data transmission rate of the incoming digital data stream ds, can in each case be selected with the aid of the fourth control signal si4.

According to a further refinement variant of the circuit arrangement, which is not illustrated in Figure 1, the loop filter LF arranged in the phase/frequency control device PLL is likewise controlled as a function of the control loop control information PLL_WORD1...n stored in the register unit REG.

The digital data stream cds sampled with the aid of the recovered clock signal ts is read to the shift register SR, that is to say the shift register SR contains the data bits read with the aid of the recovered clock ts. Alternatively, the data stream ds which is applied to the input ET but is not sampled can also be read to the shift register SR, which is clocked by the clock signal ts, via a connecting line - indicated by a dashed connecting line in Figure 1.

The bit sequence read to the shift register SR is permanently compared by the comparator unit COMP with the protocol identification information - in this case pid1 - temporarily stored in the memory register MR. If the comparator unit COMP finds a match or a partial match between the digital bit sequence that is read and the protocol identification information pid1, a corresponding control signal int is generated in the comparator unit COMP, and is transmitted via the control line SCS to the control unit STRG. The transmission of the control information int to the control unit STRG indicates the identification of the selected transmission protocol - in this case STM1 - and the setting of the associated data transmission rate for the phase/frequency control device PLL.

In order to improve the synchronization of the clock signal ts that is produced to the incoming digital data stream ds, according to a further refinement variant that is not illustrated, the control unit STRG checks whether the protocol identification information - in this case pid1 - is identified more than once, for example three times, in a cycle time which is specific for the selected transmission protocol. If the transmission protocol being used means that the frame sequence is asynchronous - for example when using the Gigabit-Ethernet transmission protocol - this refinement variant allows the pause pattern - also referred to as the "Interframe Gap" - to be analyzed.

When the selected or expected protocol identification information pid1 is identified in the sampled data stream cds, the start of data transmission can be recorded by means of the control unit STRG. If there are no periodically produced data frames - for example when using the STM-1 transmission protocol - it is advantageously possible in conjunction with further parameters - for example loss of the signal (LOS) or optical level - to deduce that there is a fault or that this is the end of transmission. In the situation where the phase locked loop which is arranged in the phase/frequency control device PLL becomes synchronized to an adjacent transmission rate - for example PDH at 140 Mbit/s - the analysis of the incoming data frames according to the invention makes it possible to identify and record the fact that the preselected transmission protocol is not being used and/or has not been identified. If, for example, the preselected transmission protocol is not identified, termination of the connection can be initiated automatically.

Automatic operation

When using the circuit arrangement illustrated in Figure 1 in the automatic operating mode, the clock

signal ts which is produced by the phase/frequency control device PLL should

be synchronized without any operator action to the digital data stream arriving at the data input ET, allowing subsequent "3D data regeneration" of the digital data stream ds. For this purpose, all the transmission protocols to be expected are stored in the table tab arranged in the memory MEM, together with the associated protocol-specific protocol identification information pid1...n and the associated control device control information PLL_WORD1...n for setting the phase/frequency control device PLL to the data transmission rate to be expected. When the automatic operating mode is activated, this causes the control unit STRG to transmit the protocol identification information PID1...n and control device control information PLL_WORD1...n arranged in the table tab of the memory MEM step-by-step in the described manner and cyclically to the register unit REG and, respectively, to the memory register MR, until the comparator unit COMP identifies a defined transmission protocol stored in the table tab, and signals this to the control unit STRG. When a transmission protocol stored in the memory MEM is identified, the cyclic processing of the table tab arranged in the memory MEM is ended. If the currently selected transmission protocol is not identified, the described, successive run through the stored protocol identification information PID1...n and control device control information PLL_WORD1...n is carried out once again, after a predefined, protocol-specific delay.

The automatic protocol search sequence can advantageously be enabled only by an operator action. According to a further advantageous refinement, selective enabling can be carried out by selection of the transmission protocols stored in the table tab by means of an appropriate identifier in the respective table entries te1...n.

In order to further improve the synchronization monitoring, the current state of the phase/frequency control device PLL can be detected with the aid of a generally known lock detector - not illustrated - which is also arranged in the phase/frequency control device PLL, and can be signaled to the control unit STRG.

The control/monitoring interface SS which is connected to the control unit STRG allows the table entries te1...n which are stored in the memory MEM to be processed and updated and, in addition to the monitoring of the respectively transmitted transmission protocols, allows the enabling of specific transmission protocols to be controlled. The control/monitoring interface SS also makes it possible to switch between the described manual or automatic operating modes. The control/monitoring interface SS can, for example, be connected to a higher-level network administration unit or network management unit so that, for example, it is possible for a network operator to monitor and to control the data transmission rate of the digital data stream ds arriving at the phase/frequency control device PLL.

The linking, according to the invention, of the presetting of the data transmission rate to be expected to the phase/frequency control device PLL (which is generally known to those skilled in the art) and the checking of the transmission protocol used for transmitting the digital data stream by partial evaluation of the overhead information contained in the individual data frames avoids false synchronization of the clock signal to side lines, harmonics and subharmonics of the data transmission rate. The method according to the invention also makes it possible to distinguish reliably between data transmission rates which are separated only slightly, by evaluation of the various overhead information items.

Patent Claims

1. A method for automatically producing clock signals (ts) for sampling data signals (ds) at different data rates by means of a phase locked loop (PLL),
characterized
in that, during a synchronization process, the data signal (cds, ds) is sampled successively using a clock signal (ts) at different frequencies, which are associated with different transmission protocols, and is checked for the presence of protocol identification information (PID1...n) associated with the selected clock signal (ts), until protocol identification information (PID1...n) is detected.

2. The method as claimed in claim 1,
characterized
in that the protocol identification information (PID1...n) is included in the overhead of a data frame.

3. The method as claimed in claim 1 or 2,
characterized
in that the protocol identification information (PID1...n) represents a pause signal.

4. The method as claimed in claim 2 or 3,
characterized
in that, once the transmission protocol being used has been detected, protocol-specific processing of at least some of the respective overhead information is carried out.

5. An arrangement for automatically producing clock signals (ts) for sampling data signals (ds), which are transmitted with the aid of transmission protocols, at different data rates, with the data signals (ds) having at least one binary protocol identification information item (PID1...n) which uniquely identifies the transmission protocol,

- having a phase locked loop (PLL) for synchronization of the clock signal (ts) to the digital data signal (ds) passed to the phase/frequency control device,
- having at least one controllable frequency divider device (T1, T2) which is arranged in the feedback path of the phase/frequency device (PLL),
- having sampling means (AFF, SR) for sampling the digital data signal (ts) with the aid of the clock signal (ts),

characterized

- in that a control unit (STRG, REG) is provided, which sets the clock signal (ts) to a frequency which corresponds to a transmission protocol,
- in that a protocol detector (RD) is provided, in which the control unit (STRG, REG) is arranged and which stores at least a portion of the sampled data signal (cds, ds) and investigates it for protocol identification information (PID1...n) and transmits the investigation result to the control unit (STRG), which, if there is no protocol identification information (PID1...n), selects further defined frequencies for the clock signal (ts) until protocol identification information (PID1...n) is identified in the sampled data signal (cds, ds).

6. The arrangement as claimed in claim 5,
characterized

- in that memory means (MEM), which are connected to the control unit (STRG, REG), are arranged in the protocol detector (RD) in order to store at least one binary protocol identification information item (PID1...n) and at least one control device control information item (PLL_WORD1...n) which is associated with the respective protocol identification information item (PID1...n) and controls the phase locked loop (PLL) on a protocol-specific basis,
- in that the control unit (STRG, REG) has means for forming at least one control signal (si1...4) from the at least one control device control information

item (PLL_WORD1...n)

which is associated with the protocol identification information item (PID1...n), with the at least one control signal (si1...4) being transmitted to the phase locked loop (PLL),

- in that detector means (SR, COMP, MR), which are connected to the control unit (SGRG, REG) are arranged in the protocol detector (RD) for detection of the stored protocol identification information (PID1...n) which is stored and is associated with the at least one control device control information item (PLL_WORD1...n) in the sampled data signal (cds, ds),
- in that the detector means (SR, COMP, MR) have signal production means for producing a control signal (int) which represents the detection result and is transmitted to the control unit (STRG, REG), and
- in that the control unit (STRG, REG) is designed such that at least one control signal (si1,3), which represents a frequency divider control information item, is formed from the at least one stored control device control information item (PLL_WORD1...n), and is transmitted to the at least one frequency divider device (T1, T2).

7. The arrangement as claimed in claim 6,
characterized
in that the control unit (STRG, REG) is designed such that, if there are a number of protocol identification information items (pid1...n) stored in the memory means (MEM), the control device control information items (PLL_WORD1...n) associated with them are transmitted successively to the phase locked loop (PLL), and the respectively associated protocol identification information items (PID1...n) are detected successively in the sampled data stream (ds, cds), with the control device control information items (PLL_WORD1...n) being transmitted successively as a function of the detection result.

8. The arrangement as claimed in claim 6 or 7, characterized

- in that the detector means (SR, COMP, MR) have
-- a shift register (SR) to which the sampled data signal or the data signal (cds, ds) and the clock signal (ts) are passed,
-- a comparator (COMP) which is connected to the shift register (SR) and to the control unit (STRG, REG), and
-- a memory register (MR), which is connected to the comparator (COMP) and to the control unit (STRG) for temporary storage of protocol identification information (PID1...n), and
- in that the comparator (COMP) is designed such that the protocol identification information (PID1...n) stored in the memory register (MR) is compared with the digital data signal (cds, ds) read to the shift register (SR), and the comparison result is transmitted to the control unit (STRG) with the aid of the control signal (int).

9. The arrangement as claimed in one of claims 6 to 8, characterized

- in that different protocol identification information items (PID1...n) and overhead control information items (CNT_WD1...n) associated with them are stored in the memory means (MEM),
- in that the sampled data signal (cds, ds) is supplied to an overhead processing unit, which is connected to the control unit (STRG, REG), for processing protocol-specific overhead information included in the data signal (cds, ds), and
- in that the overhead processing unit and the control unit (STRG, REG) are designed such that the overhead information is processed as a function of the at least one overhead control information item (CNT_WD1...n) associated with the detected transmission protocol.

10. The arrangement as claimed in one of claims 6 to 9, characterized
in that the control unit (STRG, REG) is connected to a control/monitoring interface (SS), via which

- the information (PID1...n, PLL_WORD1...n, CNT_WD1...n) stored in the memory means (MEM) can be updated, and/or
- detection results can be transmitted to a higher-level communications unit.

11. The arrangement as claimed in one of claims 6 to 10,
characterized
in that a number of voltage controlled oscillators (VCO) can be selected as a function of the control device control information (PLL_WORD1...n).

12. The arrangement as claimed in one of claims 6 to 11,
characterized
in that a frequency window discriminator (FD) is provided in the phase locked loop (PLL), which defines the frequency of the clock signal (ts) as a function of the control device control information (PLL_WORD1...n) and is likewise set by the control unit (STRG, REG).

13. The arrangement as claimed in one of claims 5 to 12,
characterized
in that a loop filter (LF) is provided in the phase locked loop (PLL), and is set by the control unit (STRG).

14. The arrangement and method as claimed in one of the preceding claims,
characterized
in that the transmission protocol represents an STM-1, STM-4, STM-16, fiber channel or Gigabit-Ethernet protocol.

Abstract

Method and arrangement for automatically producing clock signals for sampling data signals at different data rates by means of a phase locked loop

In a synchronization process by means of the phase locked loop (PLL), a data signal (cds, ds) is sampled successively using a clock signal (ts) at different frequencies, which are associated with different transmission protocols, and is checked for the presence of protocol identification information (PID1...n) associated with the selected clock signal (ts), until protocol identification information (PID1...n) is detected. The frequency resolution of the phase locked loop (PLL) is advantageously increased, and the synchronization of the clock signal (ts) to the data signal (ds) is thus improved.

FIGURE 1

FIG 1

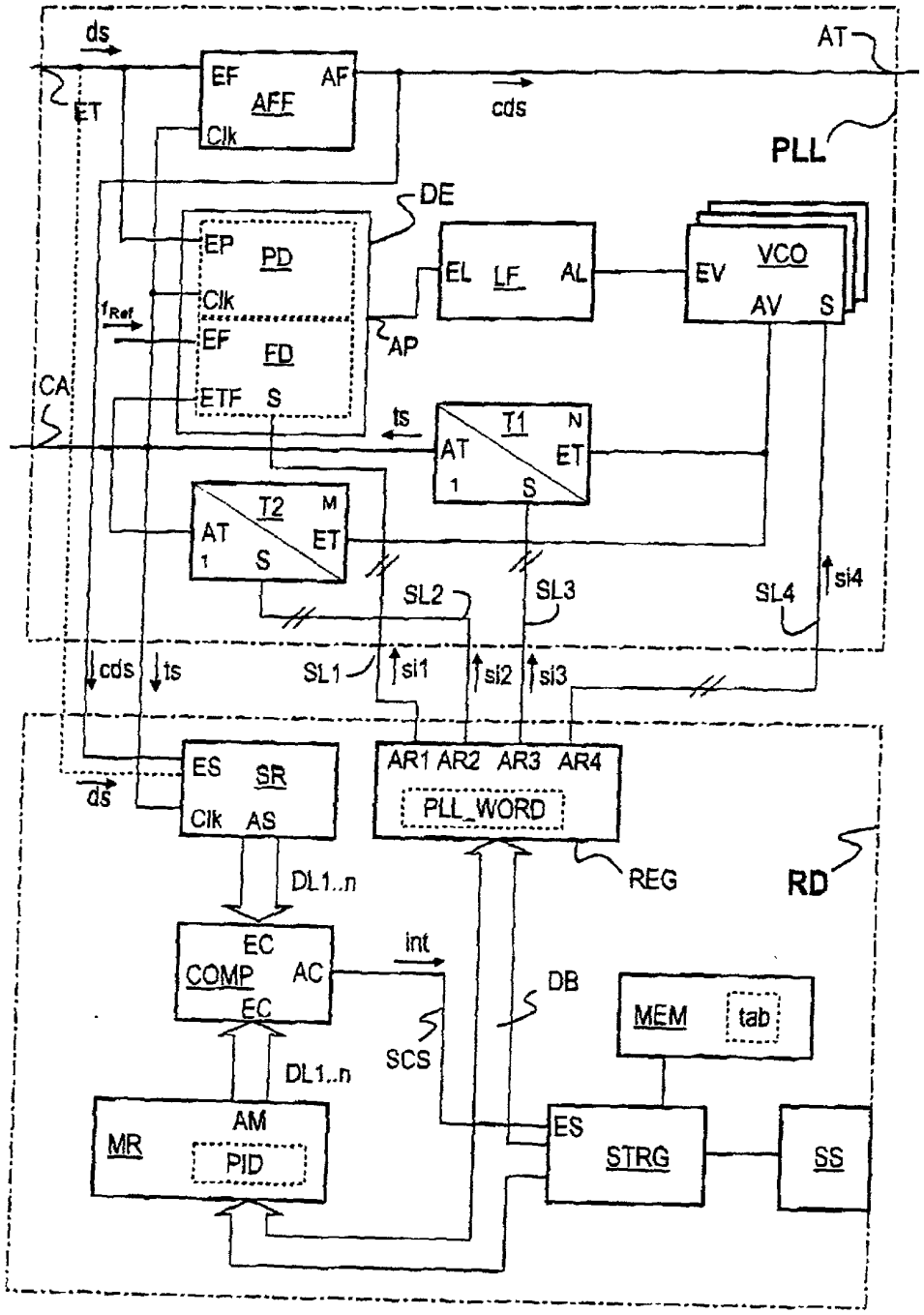
ds
AT
ET
EF
AF
AFF
Clk
cds
PLL
DE
EP
PD
Clk
EF
FD
ETF
S
EL
LF
AL
EV
VCO
AV
S
AP
f_{Ref}
CA
ts
T1
N
AT
ET
1
S
T2
M
AT
ET
1
S
SL2
SL3
SL4
si4
cds
ts
SL1
si1
si2
si3
ds
ES
SR
Clk
AS
AR1 AR2 AR3 AR4
PLL_WORD
REG
RD
DL1..n
EC
COMP
AC
EC
int
DB
MEM
tab
SCS
DL1..n
AM
MR
PID
ES
STRG
SS

FIG 2

tab

Data set No.	Transmission protocol	Protocol identification information	Control device control information	Overhead control information
te1	SDH (STM-1) (155 Mbit/s)	PID1 (e.g. A1 and A2 byte in the SOH of an SDH signal)	PLL_WORD1	CNT_WD1
te2	SDH (STM-4) (622 Mbit/s)	PID2 (e.g. A1 and A2 byte in the SOH of an SDH signal)	PLL_WORD2	CNT_WD2
te3	SDH (STM-16) (2.5 Gbit/s)	PID3 (e.g. A1 and A2 byte in the SOH of an SDH signal)	PLL_WORD3	CNT_WD3
te4	Gigabit-Ethernet (1.25 Gbit/s)	PID4 (Idle; Preamble; SFD-"Start Frame Delimiter")	PLL_WORD4	CNT_WD4
te n	....	PIDn	PLL_WORDn	CNT_WDn

Declaration and Power of Attorney For Patent Application
Erklärung Für Patentanmeldungen Mit Vollmacht
German Language Declaration

Als nachstehend benannter Erfinder erkläre ich hiermit an Eides Statt:

As a below named inventor, I hereby declare that:

dass mein Wohnsitz, meine Postanschrift, und meine Staatsangehörigkeit den im Nachstehenden nach meinem Namen aufgeführten Angaben entsprechen,

My residence, post office address and citizenship are as stated below next to my name,

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I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

Gewinnung von Taktsignalen zur Abtastung von Datensignalen unterschiedlicher Datenraten mit Hilfe eines Phasenregelkreises

Production of clock signals for sampling data signals with different rates using a phase-locking loop

deren Beschreibung

(zutreffendes ankreuzen)
☐ hier beigefügt ist.
☒ am 01.03.2000 als
PCT internationale Anmeldung
PCT Anmeldungsnummer PCT/DE00/00641
eingereicht wurde und am _____
abgeändert wurde (falls tatsächlich abgeändert).

the specification of which

(check one)
☐ is attached hereto.
☒ was filed on 01.03.2000 as
PCT international application
PCT Application No. PCT/DE00/00641
and was amended on _____
(if applicable)

Ich bestätige hiermit, dass ich den Inhalt der obigen Patentanmeldung einschliesslich der Ansprüche durchgesehen und verstanden habe, die eventuell durch einen Zusatzantrag wie oben erwähnt abgeändert wurde.

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims as amended by any amendment referred to above.

Ich erkenne meine Pflicht zur Offenbarung irgendwelcher Informationen, die für die Prüfung der vorliegenden Anmeldung in Einklang mit Absatz 37, Bundesgesetzbuch, Paragraph 1.56(a) von Wichtigkeit sind, an.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, §1.56(a).

Ich beanspruche hiermit ausländische Prioritätsvorteile gemäss Abschnitt 35 der Zivilprozessordnung der Vereinigten Staaten, Paragraph 119 aller unten angegebenen Auslandsanmeldungen für ein Patent oder eine Erfindersurkunde, und habe auch alle Auslandsanmeldungen für ein Patent oder eine Erfindersurkunde nachstehend gekennzeichnet, die ein Anmeldedatum haben, das vor dem Anmeldedatum der Anmeldung liegt, für die Priorität beansprucht wird.

I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

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Prior foreign appplications
Priorität beansprucht

			Priority Claimed	
19911464.1	DE	15.03.1999	☒	☐
(Number) (Nummer)	(Country) (Land)	(Day Month Year Filed) (Tag Monat Jahr eingereicht)	Yes Ja	No Nein
			☐	☐
(Number) (Nummer)	(Country) (Land)	(Day Month Year Filed) (Tag Monat Jahr eingereicht)	Yes Ja	No Nein
			☐	☐
(Number) (Nummer)	(Country) (Land)	(Day Month Year Filed) (Tag Monat Jahr eingereicht)	Yes Ja	No Nein

Ich beanspruche hiermit gemäss Absatz 35 der Zivilprozessordnung der Vereinigten Staaten, Paragraph 120, den Vorzug aller unten aufgeführten Anmeldungen und falls der Gegenstand aus jedem Anspruch dieser Anmeldung nicht in einer früheren amerikanischen Patentanmeldung laut dem ersten Paragraphen des Absatzes 35 der Zivilprozeßordnung der Vereinigten Staaten, Paragraph 122 offenbart ist, erkenne ich gemäss Absatz 37, Bundesgesetzbuch, Paragraph 1.56(a) meine Pflicht zur Offenbarung von Informationen an, die zwischen dem Anmeldedatum der früheren Anmeldung und dem nationalen oder PCT internationalen Anmeldedatum dieser Anmeldung bekannt geworden sind.

I hereby claim the benefit under Title 35. United States Code. §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §122, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56(a) which occured between the filing date of the prior application and the national or PCT international filing date of this application.

PCT/DE00/00641	01.03.2000	anhängig	pending
(Application Serial No.) (Anmeldeseriennummer)	(Filing Date D, M, Y) (Anmeldedatum T, M, J)	(Status) (patentiert, anhängig, aufgegeben)	(Status) (patented, pending, abandoned)
(Application Serial No.) (Anmeldeseriennummer)	(Filing Date D,M,Y) (Anmeldedatum T, M; J)	(Status) (patentiert, anhängig, aufgeben)	(Status) (patented, pending, abandoned)

Ich erkläre hiermit, dass alle von mir in der vorliegenden Erklärung gemachten Angaben nach meinem besten Wissen und Gewissen der vollen Wahrheit entsprechen, und dass ich diese eidesstattliche Erklärung in Kenntnis dessen abgebe, dass wissentlich und vorsätzlich falsche Angaben gemäss Paragraph 1001, Absatz 18 der Zivilprozessordnung der Vereinigten Staaten von Amerika mit Geldstrafe belegt und/oder Gefängnis bestraft werden koennen, und dass derartig wissentlich und vorsätzlich falsche Angaben die Gültigkeit der vorliegenden Patentanmeldung oder eines darauf erteilten Patentes gefährden können.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

German Language Declaration

VERTRETUNGSVOLLMACHT: Als benannter Erfinder beauftrage ich hiermit den nachstehend benannten Patentanwalt (oder die nachstehend benannten Patentanwälte) und/oder Patent-Agenten mit der Verfolgung der vorliegenden Patentanmeldung sowie mit der Abwicklung aller damit verbundenen Geschäfte vor dem Patent- und Warenzeichenamt: *(Name und Registrationsnummer anführen)*

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. *(list name and registration number)*

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Voller Name des einzigen oder ursprünglichen Erfinders:	Full name of sole or first inventor:
FRITZ-JOERG DAUTH	FRITZ-JOERG DAUTH
Unterschrift des Erfinders Datum	Inventor's signature Date
Fritz J. Dauth 7.9.2001	
Wohnsitz	Residence
HOLZKIRCHEN, DEUTSCHLAND DEX	HOLZKIRCHEN, GERMANY
Staatsangehörigkeit	Citizenship
DE	DE
Postanschrift	Post Office Addess
IGNAZ-GUENTHER-STR.19	IGNAZ-GUENTHER-STR.19
83607 HOLZKIRCHEN	83607 HOLZKIRCHEN
Voller Name des zweiten Miterfinders (falls zutreffend):	Full name of second joint inventor, if any:
Unterschrift des Erfinders Datum	Second Inventor's signature Date
Wohnsitz	Residence
Staatsangehörigkeit	Citizenship
Postanschrift	Post Office Address

(Bitte entsprechende Informationen und Unterschriften im Falle von dritten und weiteren Miterfindern angeben).

(Supply similar information and signature for third and subsequent joint inventors).